Reliability Evaluation of A Task Under A Hardware Fault-Tolerant Technique

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Abstract

In this work, we discuss an efficient fault-tolerant technique that is devised to ensure the generation of correct outputs for tasks despite of processors and communication links failures. We also estimate a lower bound for the reliability of a task under the above technique.

1 INTRODUCTION

Hardware fault-tolerance for tolerating processors and communication links failures can be achieved by using one of the two following approaches:

1. *Comparison model*: Fault tolerance is achieved by masking the effects of the faults. Traditionally, masking faults has been implemented with the employment of *N-Modular Redundancy (NMR)* technique at the cost of resources utilization. The basic concept of NMR is to use N (usually an odd number) processors to run the same task and then perform a majority vote to determine the output for the task. For example to mask t faulty processors we need at least $(2t + 1)$ processors, so when the majority vote takes place the $(t + 1)$ fault-free processors will outvote the outputs of the faulty processors. Variations of this technique have been employed earlier [1] - [4].

2. *Testing model*: Fault-Tolerance is achieved by the following ordered steps: faults detection, fault location, system reconfiguration and error recovery. Fault detection and fault location are achieved by assigning processors to test each others and analyzing the outcomes [5] - [12].

Testing model requires processors run diagnostic programs on each others for the purpose of fault detection. Diagnostic programs require faults to be modeled properly; otherwise, fault coverage of the diagnostic programs may not be very high.